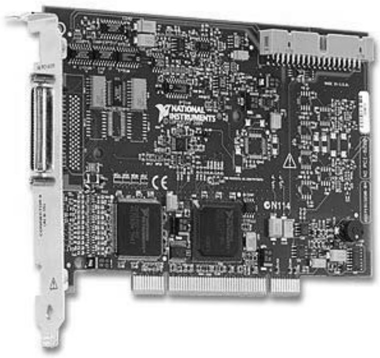
Low-Cost M Series Multifunction Data Acquisition - 16-Bit, 250 kS/s, up to 80 Analog Inputs



NI recommends high-speed M Series (NI 625x) for 5X faster sampling rates, high-accuracy M Series (NI 628x) for 4X higher resolution, or industrial M Series (NI 623x) for 60 VDC isolation and superior noise rejection // 16, 32, or 80 analog inputs at 16 bits, 250 kS/s
Up to 4 analog outputs at 16 bits, 833 kS/s (6 µs full-scale settling time)
Programmable input range (±10, ±5, ±1, ±0.2 V) per channel
Up to 48 TTL/CMOS digital I/O lines (up to 32 hardware-timed at 1 MHz)
Two 32-bit, 80 MHz counter/timers // Digital triggering
///// X1, X2, or X4 quadrature encoder inputs

Analog Input	
Number of channels	
NI 6220/6221	8 differential or 16 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the *AI Absolute Accuracy Table*
Sampling rate	
Maximum	250 kS/s single channel, 250 kS/s multi-channel (aggregate)
Minimum	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Input coupling	DC
Input range	±10 V, ±5 V, ±1 V, ±0.2 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	92 dB
Input impedance	
Device on	
AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI- to AI GND	>10 GΩ in parallel with 100 pF
Device off	

AI+ to AI GND	820 Ω
AI- to AI GND	820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	-75 dB
Non-adjacent channels	-90 dB[1]
Small signal bandwidth (-3 dB)	700 kHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	
PCI/PXI devices	DMA (scatter-gather), interrupts, programmed I/O
Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2)	
Device on	±25 V for up to two AI pins
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA max/AI pin

Analog Output
Back to Detailed Specs

Number of channels	
NI 6220/6224	0
NI 6221/6225	2
NI 6229	4
DAC resolution	16 bits
DNL	±1 LSB
Monotonicity	16 bit guaranteed
Maximum update rate	
1 channel	833 kS/s
2 channels	740 kS/s per channel
3 channels	666 kS/s per channel
4 channels	625 kS/s per channel
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Output range	±10 V
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	10 mA
Power-on state	±20 mV[2]
Power-on glitch	400 mV for 200 ms

Output FIFO size	8,191 samples shared among channels used
Data transfers	
PCI/PXI devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O
AO waveform modes: Non-periodic waveform Periodic waveform regeneration mode from onboard FIFO Periodic waveform regeneration from host buffer including dynamic update	
Settling time, full scale step 15 ppm (1 LSB)	6 µs
Slew rate	15 V/µs
Glitch energy	
Magnitude	100 mV
Duration	2.6 µs

Calibration (AI and AO)

Back to Detailed Specs

Recommended warm-up time	15 minutes
Calibration interval	1 year

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale[1] (µV)	Sensitivity[2] (µV)
Positive Full Scale	Negative Full Scale									
10	-10	75	25	5	20	57	76	244	3,100	97.6
5	-5	85	25	5	20	60	76	122	1,620	48.8
1	-1	95	25	5	25	79	76	30	360	12.0
0.2	-0.2	135	25	5	80	175	76	13	112	5.2

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty
GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

$$\text{NoiseUncertainty} = \frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$$ For a coverage factor of 3 σ and averaging 100 points.

[1] Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:
TempChangeFromLastExternalCal = 10 °C
TempChangeFromLastInternalCal = 1 °C
number_of_readings = 100
CoverageFactor = 3 σ
For example, on the 10 V range, the absolute accuracy at full scale is as follows:
GainError = 75 ppm + 25 ppm · 1 + 5 ppm · 10 GainError = 150 ppm
OffsetError = 20 ppm + 57 ppm · 1 + 76 ppm OffsetError = 153 ppm

$$\text{NoiseUncertainty} = \frac{244\ \mu V \cdot 3}{\sqrt{100}} \qquad \text{NoiseUncertainty} = 73\ \mu V$$

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 3,100 µV
[2] Sensitivity is the smallest voltage change that can be detected. It is a function of noise.
Accuracies listed are valid for up to one year from the device external calibration.

AO Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale[1] (µV)
Positive Full Scale	Negative Full Scale							
10	-10	90	10	5	40	5	128	3,230

[1] Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration. Accuracies listed are valid for up to one year from the device external calibration.

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualOffsetError + AOOffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

ANALOG DEVICES

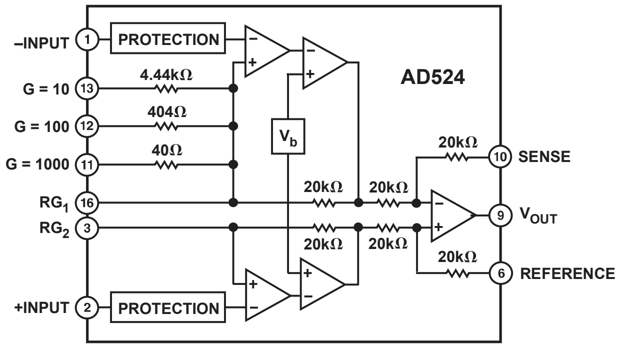
Precision Instrumentation Amplifier

AD524

FEATURES

Low Noise: 0.3 μV p-p 0.1 Hz to 10 Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120 dB (G = 1000)
Low Offset Voltage: 50 μV
Low Offset Voltage Drift: 0.5 μV/°C
Gain Bandwidth Product: 25 MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On–Power Off
No External Components Required
Internally Compensated
MIL-STD-883B and Chips Available
16-Lead Ceramic DIP and SOIC Packages and 20-Terminal Leadless Chip Carriers Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Standard Military Drawing Also Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25 μV/°C, input offset voltage drift of less than 0.5 μV/°C, CMR above 90 dB at unity gain (120 dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications, the AD524 also has a 25 kHz gain bandwidth product (G = 1000). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5 V/μs and settles in 15 μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power-on and power-off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical “A” grade, the low drift “B” grade and lower drift, higher linearity “C” grade are specified from –25°C to +85°C. The “S” grade guarantees performance to specification over the extended temperature range –55°C to +125°C. Devices are available in 16-lead ceramic DIP and SOIC packages and a 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power-on and power-off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25 MHz, full power response of 75 kHz and a settling time of 15 μs to 0.01% of a 20 V step (G = 100).

REV. E

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD524–SPECIFICATIONS (@ $V_S = \pm15$ V, $R_L = 2$ kΩ and $T_A = +25°C$ unless otherwise noted)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error[1]													
G = 1			**±0.05**			**±0.03**			**±0.02**			**±0.05**	%
G = 10			**±0.25**			**±0.15**			**±0.1**			**±0.25**	%
G = 100			**±0.5**			**±0.35**			**±0.25**			**±0.5**	%
G = 1000			**±2.0**			**±1.0**			**±0.5**			**±2.0**	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10,100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			**250**			**100**			**50**			**100**	µV
vs. Temperature			2			**0.75**			**0.5**			**2.0**	µV/°C
Output Offset Voltage			5			**3**			**2.0**			**3.0**	mV
vs. Temperature			100			**50**			**25**			**50**	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	**70**			**75**			**80**			**75**			dB
G = 10	**85**			**95**			**100**			**95**			dB
G = 100	**95**			**105**			**110**			**105**			dB
G = 1000	**100**			**110**			**115**			**110**			dB
INPUT CURRENT													
Input Bias Current			**±50**			**±25**			**±15**			**±50**	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			**±35**			**±15**			**±10**			**±35**	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DL})[2]	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})	$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			V
Common-Mode Rejection dc to 60 Hz with 1 kΩ Source Imbalance													
G = 1	**70**			**75**			**80**			**70**			dB
G = 10	**90**			**95**			**100**			**90**			dB
G = 100	**100**			**105**			**110**			**100**			dB
G = 1000	**110**			**115**			**120**			**110**			dB
OUTPUT RATING													
V_{OUT}, $R_L = 2$ kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal – 3 dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step													
G = 1 to 100		15			15			15			15		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1 kHz													
R.T.I.		7			7			7			7		nV/√Hz
R.T.O.		90			90			90			90		nV√Hz
R.T.I., 0.1 Hz to 10 Hz													
G = 1		15			15			15			15		µV p-p
G = 10		2			2			2			2		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1 Hz to 10 Hz		60			60			60			60		pA p-p

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	–25		+85	–25		+85	–25		+85	–55		+125	°C
Storage	–65		+150	–65		+150	–65		+150	–65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA

NOTES
[1]Does not include effects of external resistor R_G.
[2]V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at the maximum = 10 V/G.
V_D = Actual differential input voltage.
Example: G = 10, V_D = 0.50.
V_{CM} = 12 V – (10/2 × 0.50 V) = 9.5 V.

Specification subject to change without notice.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

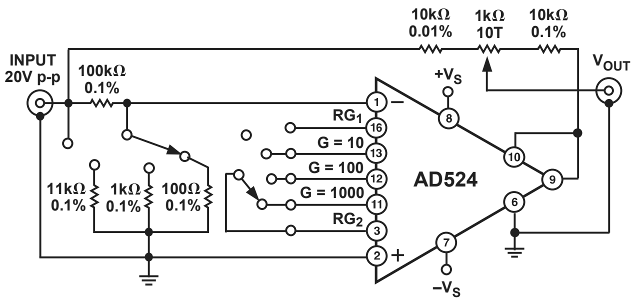


Figure 27. Settling Time Test Circuit

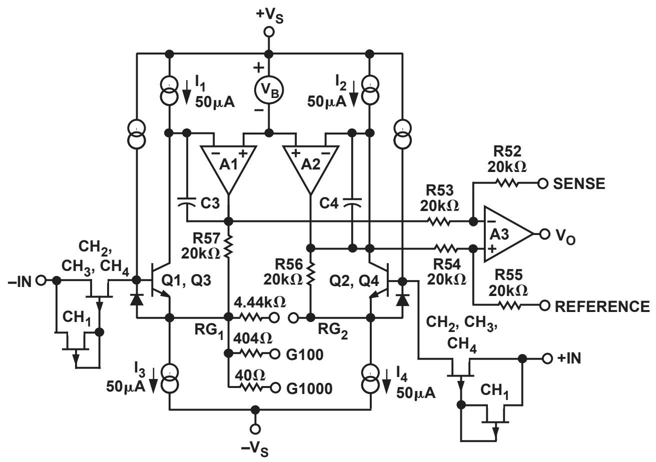


Figure 28 Simplified Circuit of Amplifier; Gain Is Defined as ((R56 + R57)/(R_G)) + 1. For a Gain of 1, R_G Is an Open Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant, which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000, thus reducing gain-related errors to a negligible 30 ppm. Second, the gain bandwidth product, which is determined by C3 or C4 and the input transconductance, reaches 25 MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of 7 $nV/\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5 mA with a full differential overload (36 V) would require over 7k of resistance which would add 10 $nV\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance (≈1 kΩ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance (≈3 kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3 mA over the 36 V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an autozero cycle, but there are many small-signal high-gain applications that don't have this capability.

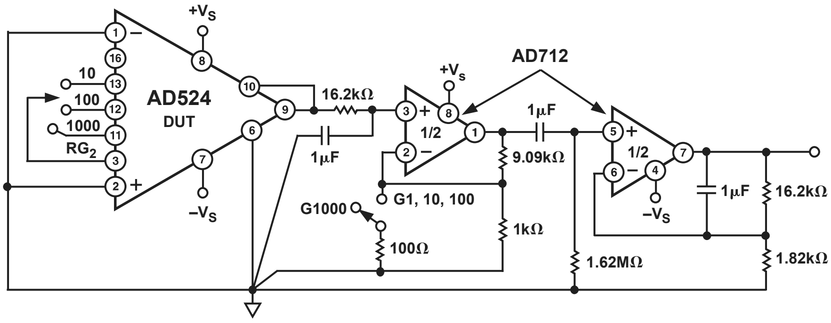


Figure 29. Noise Test Circuit

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250 µV output offset and a –50 µV input offset. In a unity gain configuration, the *total* output offset would be 200 µV or the sum of the two. At a gain of 100, the output offset would be –4.75 mV or: +250 µV + 100(–50 µV) = –4.75 mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G = 1 RG_2 is not connected).

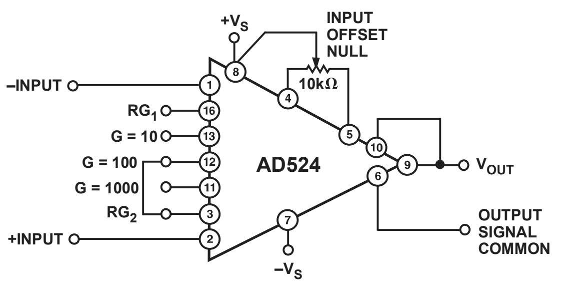


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16, which programs the gain according to the formula

$$R_G = \frac{40k}{G = -1}$$

(see Figure 31).

For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (– 50 ppm/°C typ).

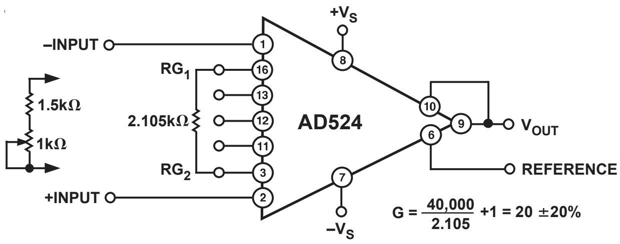


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

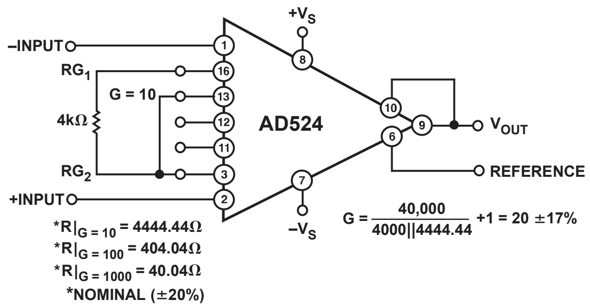


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

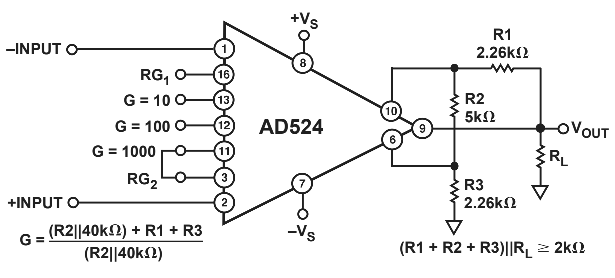


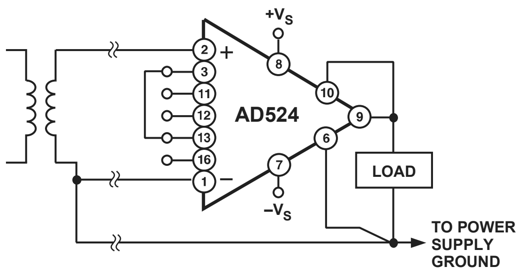
Figure 33. Gain of 2000

Table I. Output Gain Resistor Values

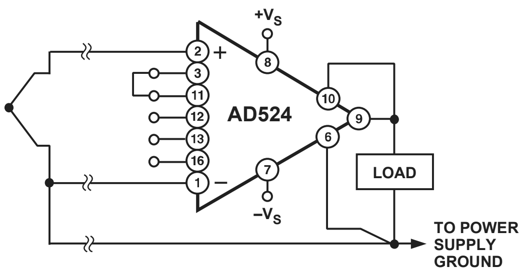
Output Gain	R2	R1, R3	Nominal Gain
2	5 kΩ	2.26 kΩ	2.02
5	1.05 kΩ	2.05 kΩ	5.01
10	1 kΩ	4.42 kΩ	10.1

INPUT BIAS CURRENTS

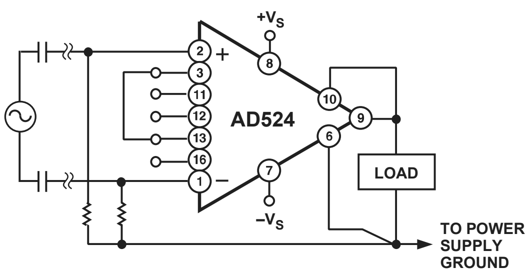
Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in a total error budget. The bias currents, when multiplied by the source resistance, appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards that are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

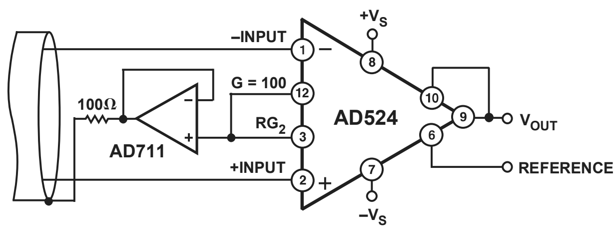


Figure 35. Shield Driver, G ≥ 100

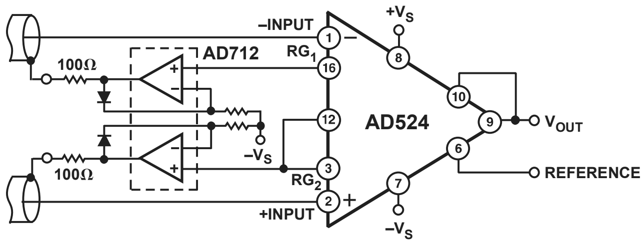


Figure 36. Differential Shield Driver

GROUNDING

Many data acquisition components have two or more ground pins that are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100 Ω, supplying a 0 to 20 mV signal to an AD524C. The output of the IA feeds a 14-bit A-to-D converter with a 0 to 2 volt input voltage range. The operating temperature range is –25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C – 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45 ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A-to-D output, the addition of a autogain/autozero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

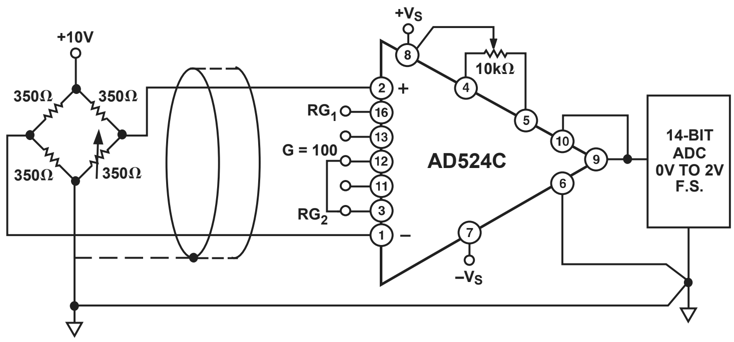


Figure 46. Typical Bridge Application

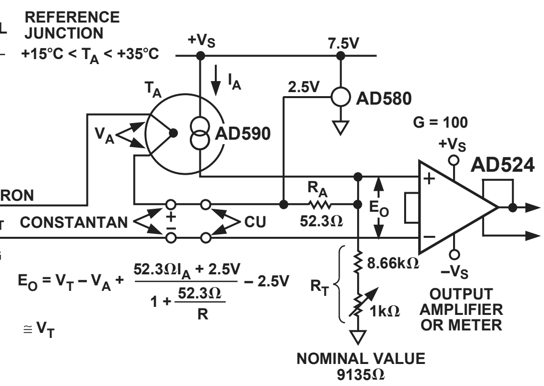
Table II. Error Budget Analysis of AD524CD in Bridge Application

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = +25°C	Effect on Absolute Accuracy at T_A = +85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500 ppm	2500 ppm	2500 ppm	–
Gain Instability	25 ppm	(25 ppm/°C)(60°C) = 1500 ppm	–	1500 ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30 ppm	–	–	30 ppm
Input Offset Voltage	±50 µV, RTI	±50 µV/20 mV = ±2500 ppm	2500 ppm	2500 ppm	–
Input Offset Voltage Drift	±0.5 µV/°C –	(±0.5 µV/°C)(60°C) = 30 µV 30 µV/20 mV = 1500 ppm	–	1500 ppm	–
Output Offset Voltage*	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	–
Output Offset Voltage Drift*	±25 µV/°C	(±25 µV/°C)(60°C)= 1500 µV 1500 µV/20 mV = 750 ppm	–	750 ppm	–
Bias Current-Source Imbalance Error	±15 nA	(±15 nA)(100 Ω) = 1.5 µV 1.5 µV/20 mV = 75 ppm	75 ppm	75 ppm	–
Bias Current-Source Imbalance Drift	±100 pA/°C	(±100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV= 30 ppm	–	30 ppm	–
Offset Current-Source Imbalance Error	±10 nA	(±10 nA)(100 Ω) = 1 µV 1 µV/20 mV = 50 ppm	50 ppm	50 ppm	–
Offset Current-Source Imbalance Drift	±100 pA/°C	(100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV = 30 ppm	–	30 ppm	–
Offset Current-Source Resistance-Error	±10 nA	(10 nA)(175 Ω) = 3.5 µV 3.5 µV/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	–
Offset Current-Source Resistance-Drift	±100 pA/°C	(100 pA/°C)(175 Ω)(60°C) = 1 µV 1 µV/20 mV = 50 ppm	–	50 ppm	–
Common Mode Rejection 5 V dc	115 dB	115 dB = 1.8 ppm × 5 V = 8.8 µV 8.8 µV/20 mV = 444 ppm	444 ppm	444 ppm	–
Noise, RTI (0.1 Hz–10 Hz)	0.3 µV p-p	0.3 µV p-p/20 mV = 15 ppm	–	–	15 ppm
		Total Error	6656.5 ppm	10516.5 ppm	45 ppm

*Output offset voltage and output offset voltage drift are given as RTI figures.

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple-iron(+)–constantan–is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

TYPE	R_A NOMINAL VALUE
J	52.3Ω
K	41.2Ω
E	61.4Ω
T	40.2Ω
S, R	5.76Ω



$$E_O = V_T - V_A + \frac{52.3\Omega I_A + 2.5V}{1 + \frac{52.3\Omega}{R}} - 2.5V$$

$$\cong V_T$$

Figure 47. Cold-Junction Compensation

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

The microprocessor controlled data acquisition system shown in Figure 48 includes both autozero and autogain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The autozero cycle, in this application, converts a number that appears to be ground and then writes that same number (8-bit) to the AD7524, which eliminates the zero error since its output has an inverted scale. The autogain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

For a comprehensive study of instrumentation amplifier design and applications, refer to the *Instrumentation Amplifier Application Guide,* available free from Analog Devices.

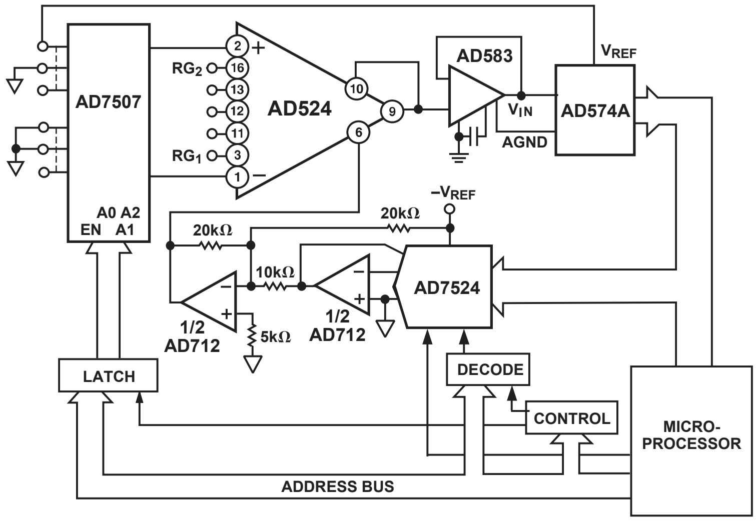


Figure 48. Microprocessor Controlled Data Acquisition System